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Γ	APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	•
	10/674,693	09/30/2003	Sherman Lee	50915/SDB/B600	5114	•
	23363	23363 7590 09/22/2005		EXAMINER		
	CHRISTIE, F PO BOX 7068	PARKER & HALE, LI	LP .	NGUYE	N, LEE	
		CA 91109-7068		ART UNIT	PAPER NUMBER	
	·			2682		

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)					
	10/674,693	LEE ET AL.					
Office Action Summary	Examiner	Art Unit					
	LEE NGUYEN	2682					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status							
1) Responsive to communication(s) filed on	Responsive to communication(s) filed on						
2a) ☐ This action is <b>FINAL</b> . 2b) ☒ This	action is non-final.						
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.							
Disposition of Claims							
4) ☐ Claim(s) 1-27 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration.  5) ☐ Claim(s) is/are allowed.  6) ☐ Claim(s) 1,2,4-15 and 17-27 is/are rejected.  7) ☐ Claim(s) 3 and 16 is/are objected to.  8) ☐ Claim(s) are subject to restriction and/or election requirement.							
Application Papers							
9) The specification is objected to by the Examiner.							
10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority under 35 U.S.C. § 119							
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No.</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>							
Attachment(s)							
1) Notice of References Cited (PTO-892)	4) Interview Summary						
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	Paper No(s)/Mail Da						

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#### **DETAILED ACTION**

#### Information Disclosure Statement

1. The IDS filed 9/30/03 and 2/25/05 have been considered and recorded in the file.

#### Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-2, 4-15, 17-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rieger, III (US Patent 5,732,324) in view of Banu et al. (US 5,757,872).

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Regarding claim 1, Rieger teaches a wireless receiver (fig. 1), comprising: a receiver 2 that receives a wireless signal; a demodulator 2, 3 coupled to the receiver 2, the demodulator 2, 3 recovering a data signal and at least one clock signal from at least one signal output by the receiver circuit 2 (see data stream, clock in col. 6, lines 9-20); a computer 6 configured to generate a read signal (see reading, col. 6, line 18) and a first-in first-out memory 5 coupled to the demodulator 2, 3 to receive the data signal and the at least one clock signal. Rieger fails to teach that the first-in first-out memory 5 stores the data signal in response to the at least one clock signal. Banu teaches that that the first-in first-out memory 210 (fig. 2) stores the data signal 212 in response to the at least one clock signal 209 (col. 2, lines 31-34 and 46-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Banu with Rieger in order to help alleviate the problems of frequency mismatch and jitter. Rieger also teaches that the first-in first-out memory 5 is coupled to the computer 6 to receive the read signal (fig. 1 of Rieger).

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Regarding claim 2, the combination of Rieger and Banu also teaches that the read signal is synchronized with a computer clock signal 3 (fig. 1, col. 6, lines 16-19 of Rieger).

Regarding claim 4, Rieger inherently teaches that the computer 6 operates at a higher speed than the at least one clock signal since it has to synchronize with many differently received clock signals.

Regarding claim 5, Rieger also teaches that computer reads the data signal from the first-in first-out memory in bursts (see fig. 3b, burst audio data of Rieger).

Regarding claims 6-8, Rieger and Banu fails to teach that the first-in first-out memory sized accordance with a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory read, or in accordance with a length of data transmitted, or in accordance with a product

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of a length of data transmitted and a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory read. However, adapting a size for a memory is just a choice for a designer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the memory size of Rieger and Banu with respected sizes in accordance with required applications.

Regarding claim 9, Rieger teaches a wireless receiver (fig. 1), comprising: a receiver 2 that receives a wireless signal; a demodulator coupled to the receiver, the demodulator 2, 3 recovering a data signal and at least one clock signal from at least one signal output by the receiver circuit (see data stream, clock in col. 6, lines 9-20); a first first-in first-out memory 5 coupled to the demodulator 2, 3 to receive the data signal and the at least one clock signal. Rieger fails to teach that the first-in first-out memory 5 stores the data signal in response to the at least one clock signal. Banu teaches that that the first-in first-out memory 210 (fig. 2) stores the data signal 212 in response to the at least one clock signal 209 (col. 2, lines 31-34 and 46-

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50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Banu with Rieger in order to help alleviate the problems of frequency mismatch and jitter. Rieger also teaches that the first-in first-out memory 5 is coupled to the computer 6 to receive the read signal (fig. 1 of Rieger). Rieger also teaches a data processor 6 configured to generate the read signal (reading, col. 6, line 18) and coupled the first first-in first-out memory 5 to receive the data signal, the data processor comprising RAM 8 a second first-in first-out memory for storing the data signal received from the first first-in first-out data memory 5. However, Rieger fails to teach that the RAM 8 is a first-in first-out memory. It is taken official notice that a RAM with a first in first out category is conventionally well known. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a FIFO RAM into the wireless receiver of Rieger and Banu because FIFO can be easily realized in RAM.

Regarding claim 10, Rieger inherently teaches a computer coupled to the data processor to receive the data signal stored in the second first-in first-out memory (see modem 17 in figure 1 of Rieger).

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Regarding claim 11, Rieger also teaches that the computer sends signal to the data processor to receive the data signal stored in the second first-in first-out memory (col. 6, lines 32-34 of Rieger).

Regarding claim 12, Rieger also teaches that the data processor reads the data signal from the first first-in first-out memory in bursts (see fig. 3b, burst audio data of Rieger).

Regarding claim 13, Rieger inherently teaches that data processor reads the data signal from the first first-in first-out memory at a constant rate (see col. 4, lines 58-59 of Rieger, 2 million audio samples per second).

Regarding claim 14, the method claim is interpreted and rejected for the same reason as set forth in apparatus claim 1.

Regarding claim 15, the method claim is interpreted and rejected for the same reason as set forth in apparatus claim 2.

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Regarding claim 17, the method claim is interpreted and rejected for the same reason as set forth in apparatus claim 4.

Regarding claim 18, the method claim is interpreted and rejected for the same reason as set forth in apparatus claim 5.

Regarding claims 19-21, the method claims are interpreted and rejected for the same reason as set forth in apparatus claims 6-8.

Regarding claim 22, the method claim is interpreted and rejected for the same reason as set forth in apparatus claim 9.

Regarding claim 23, the method claim is interpreted and rejected for the same reason as set forth in apparatus claim 10.

Regarding claims 24-25, the method claims are interpreted and rejected for the same reason as set forth in apparatus claim 11.

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Regarding claim 26, the method claim is interpreted and rejected for the same reason as set forth in apparatus claim 12.

Regarding claim 27, the method claim is interpreted and rejected for the same reason as set forth in apparatus claim 13.

### **Double Patenting**

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-2 and 14-15 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 of U.S. Patent No. 6,650,880). Although the conflicting claims are not identical, they are not patentably distinct from each other because:

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Regarding claims 1-2 and 15-16, claim 1 of U.S. Patent'880 encompasses all the limitations as claimed. Furthermore, the read signal reads on the second clock signal.

## Allowable Subject Matter

5. Claims 3 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 3 and 16, the prior art of record fails to teach that computer reads the data signal from the first-in first-out memory without synchronizing a clock to the at least one clock signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEE NGUYEN whose telephone number is 571-272-7854. The examiner can normally be reached on FIRST FRIDAY OFF.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NICK CORSARO can be reached on 571-272-7856. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PRIMARY EXAMINER